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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,134	09/04/2001	Mitsugu Kusunoki	500.40612X00	2325

20457 7590 01/10/2005

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/944,134	Applicant(s) KUSUNOKI, MITSUGU	
	Examiner Juan A. Torres	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *1-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11192004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement filed on 09/04/2001 does not fully comply with the requirements of 37 CFR 1.98 because: doesn't use the USPTO forms PTO/SB/08a and PTO/SB/08b or its equivalent PTO 1449 (these forms can be obtained in http://www.uspto.gov/web/forms/index.html, attached to this office action are also these forms). Attached is a PTO/SB/08a and PTO/SB/08b forms filled by the examiner.

Drawings

The drawings are objected to because.

In FIG.3 the dot block shall be marked as 230 as referenced in the specification page 29 line 18.

In FIG. 5 the notation "C1" below the first PLL block should be "C1A" as described in the specification page 20 line 3.

In FIG. 5 the notations "1F83" "1F84" are missing in the block CB4A as described in the specification page 21 line 10.

In FIG. 6 block 448 is not shown and it is described in several places of the specification page 24 line 16, page 25 line 21.

In FIG. 6 block 111b is not shown and it is described in several places of the specification page 23 lines 15, 16 and 23, page 24 line 12.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

In page 16 lines 9 and 10 the recitation "compared with the the case" is suggested to be changed to "compared with the case".

In page 21 line 9 the recitation "CB1 to CB4" is suggested to be changed to "CB1A to CB4A", as it is described in FIG. 5.

In page 21 line 10 the recitation "I/F81 to I/F84 is not shown in FIG. 5.

In page 21 line 10 the recitation "1114b" is suggested to be changed to "114b" as it is shown in FIG. 5.

In page 22 line 2 the recitation "CB1 to CB4" is suggested to be changed to "CB1A to CB4A", as it is described in FIG. 5.

In page 22 line 6 the recitation "CB1 to CB4" is suggested to be changed to "CB1A to CB4A", as it is described in FIG. 5.

In page 22 line 13 the recitation "CB1 to CB4" is suggested to be changed to "CB1A to CB4A", as it is described in FIG. 5.

In page 23 line 15 the recitation "111b" is not shown in FIG. 6.

In page 23 line 16 the recitation "111b" is not shown in FIG. 6.

In page 23 line 23 the recitation "111b" is not shown in FIG. 6.

In page 24 line 12 the recitation "111b" is not shown in FIG. 6.

In page 24 line 16 the recitation "448" is not shown in FIG. 6.

In page 25 line 4 the recitation "CKENO" is suggested to be changed to "CKEN0" as shown in FIG. 5.

In page 25 line 21 the recitation "448" is not shown in FIG. 6.

In page 26 line 20 the recitation "111b" is not shown in FIG. 6.

In page 32 line 28 the recitation "44y" is suggested to be changed to "447" as indicated in page 32 line 24.

In page 35 line 8 the recitation "VDD" is suggested to be changed to "Vdd" as shown in FIG. 12C.

In page 35 line 10 the recitation "VSS" is suggested to be changed to "Vss" as shown in FIG. 12C.

Appropriate correction is required.

Claim Objections

Claims 1-11 are objected to because of the following informalities: in line 6 of claim 1 the recitation "said first circuit" is ambiguous because there are not antecedent to said recitation in the claim, it is suggested to be changed to "a first circuit".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 11 of claim 1 the recitation "said second signal path" is vague and indefinite. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (JP 05159080), and further in view of Isobe et al. (US 6078623).

As per claim 1 Takahashi et al. (JP 05159080) disclose a semiconductor integrated circuit comprising: a plurality of circuit blocks each having a clock distribution line pattern (figure 1 blocks 10a to 10d paragraph [0008]); where the circuit blocks are formed on a single semiconductor substrate (figure 1 blocks 10a to 10d paragraph [0008]); and where the first and second signal paths have substantially the same wiring conductor length (figure 4 paragraph [0013]). Takahashi et al. (JP 05159080) don't disclose the details of the clock and data transmission paths between the different blocks. Isobe et al. (US 6078623) disclose the data and clock transmission paths between two different circuit blocks, with a first signal path for transmitting a data signal from a first circuit block to a second circuit block (figure 13 block 92); and at least a first buffer circuit connected to the first signal path in such a manner as to constitute the first signal path and at least a second buffer circuit connected to the second signal path in such a manner as to constitute the second signal path (figure 13 blocks 92-16-26 and blocks 91-3 column 13 lines 62-65); where the clock signal and the data signal are transmitted in parallel to each other (figure 13 blocks 90 92 and 91 column 13 line 46-47). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP

05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 2 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also disclose an output latch circuit for latching the data signal to be transmitted, the second circuit block has an input latch circuit for latching the data signal to be received, and the output latch circuit and the input latch circuit are configured to perform the latch operation in response to the clock signals before and after, respectively, being transmitted from the first circuit block to the second circuit block (figure 13 blocks 11, 15, 25 and 21 column 14 line 7-9). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 3 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also disclose a first circuit block that is configured to send the next data signal and the clock signal to the first and second signal paths before arrival of the transmitted data signal clock signal at the second

circuit block (figure 13 column 14 line 3-7). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 4 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Takahashi et al. (JP 05159080) also disclose that the second circuit block includes a plurality of circuits operated in synchronism with the internal clock generated based on the clock signal received from the second signal path, and the clock distribution line pattern of the second circuit block is configured to distribute the internal clock to the plurality of circuits through the substantially same length of path (figure 1 blocks 10a to 10d paragraph [0009]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 5 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also disclose that the circuit blocks are configured in such a manner that when the data signal is not sent out to the second circuit block from the first circuit block, the clock signal is not sent out from the first circuit block to the second circuit block (figure 13 blocks 11, 15, 25 and 21 column 14 line 7-9). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 6 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Takahashi et al. (JP 05159080) also disclose that a third signal for feeding back the clock signal received by the second circuit block to the first circuit block is inserted between the first and second circuit blocks, and the first circuit block includes a phase adjusting circuit for adjusting the phase of the clock signal sent out from the first circuit block in such a manner that the clock signal in the first circuit block is in phase with the clock signal fed back (figure 3 paragraph [0011]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been

obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 7 Takahashi et al. (JP 05159080) also disclose that a phase adjusting circuit includes a phase detecting circuit for generating a phase difference signal representing the phase difference obtained by comparing the phase of the clock signal in the first circuit block with the phase of the clock signal fed back, and variable delay circuits with the delay time thereof variable based on the phase difference signal from the phase detecting circuit (figure 3 blocks 31-33 paragraph [0011] and [0012]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 8 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Takahashi et al. (JP 05159080) also disclose that the second circuit

block includes a plurality of circuits operated in synchronism with a clock signal different from the clock signal received, and the clock distribution line pattern of the second circuit block is configured to distribute different clock signal to a plurality of the circuits through paths having substantially the same length (figure 1 paragraph [0010]). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 9 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the second circuit block includes means for taking the serial data signal received from the first signal path, based on the received clock signal and storing the serial data signal for at least two periods of the received clock signal, and means for reading the data signal stored in the storage means by a clock signal different from the received clock signal (figure 14 block 102 and 103, column 14 lines 18-19). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US

6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 10 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the second circuit block includes a phase shifting circuit for generating a clock signal out of phase by one half period of the data transmission cycle based on the received clock, and a phase adjusting circuit for generating a clock signal giving a timing of taking data to the holding means based on the clock signal generated by the phase shifting circuit, and where the phase adjusting circuit operates to adjust the phase of the clock signal supplied to the holding means in such a manner that the clock signal generated by the phase-shifting circuit is in phase with the phase of the clock signal supplied to the holding means (figure 14 blocks 26, 21, 22 25 and 40, column 13 lines 54-62). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

As per claim 11 Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teach claim 1. Isobe et al. (US 6078623) also teach that the holding means is configured to take the received data signal substantially at the center between the changing points of the received data signal (figure 14 blocks 26, 21, 22 25 and 40, column 14 lines 7-9). Takahashi et al. (JP 05159080) and Isobe et al. (US 6078623) teachings are analogous art because they are from the similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the data transmission apparatus disclosed by Isobe et al. (US 6078623) in the integrated circuit with a clock distribution system disclosed by Takahashi et al. (JP 05159080). The suggestion/motivation for doing so would have been to ensure the transmission of data between the blocks different units using a low cost hardware implementation (Isobe et al. (US 6078623) abstract).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Parry et all (US 6680636) disclose a clock edge placement circuit for implementing source synchronous communication between integrated circuit devices. The clock edge placement circuit includes a delay line having an input to receive a clock signal from an external clock source. A corresponding output is included to provide the clock signal to external logic elements. The delay line structure adapted to add a propagation delay to the input, wherein the propagation delay is sized such that the phase of the clock signal is adjusted to control synchronous sampling by the external logic elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT 12-2-2004

M. G

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER